Amendments to the claims (this listing replaces all prior listings):

1. (Currently amended) Apparatus comprising:

a cache memory comprising cache lines to store data, at least a portion of the data to be written to a main memory, ~~the cache memory complying with a cache coherent protocol~~; and

an eviction mechanism to evict data stored in one of the cache lines based on validity state information associated with the data stored in the ~~one~~ cache line, the eviction mechanism to send the evicted data to the main memory.

2. (Currently amended) The apparatus of claim 1 in which each of the cache lines is to store data that corresponds to consecutive addresses in ~~a main~~ the main memory.

3. (Original) The apparatus of claim 1 in which each cache line has multiple portions.

4. (Previously Presented) The apparatus of claim 3 further comprising a storage to store validity bits that track the validity of respective portions of the cache line.

5. (Original) The apparatus of claim 4 in which the validity bits are set to a predefined value to indicate that the respective portion has been written in full in one write transaction.

6. (Previously Presented) The apparatus of claim 5 in which the eviction mechanism is to evict the cache line when the validity bits all have the predefined value.

7. (Previously Presented) The apparatus of claim 1 in which the eviction mechanism is to evict the data even if the cache is not full and data in other cache lines is not being evicted at the same time.

8. (Currently amended) The apparatus of claim 1, further comprising ~~a memory~~the main memory to store the data evicted by the eviction mechanism.

9. (Previously Presented) The apparatus of claim 8, further comprising an input/output device that generates the data stored in the cache memory.

10. (Currently amended) Apparatus comprising:

cache lines, each to store bytes of data that correspond to consecutive addresses in a main memory, at least a portion of the data to be written to the main memory, each cache line corresponding to a group of validity bits, each of the validity bits tracking a portion of the cache line and being set to a predefined value when the tracked portion of the cache line is fully written with new data in one write transaction~~, the cache lines complying with a cache coherent protocol~~; and

an eviction component to evict the bytes of data stored in one of the cache lines when the group of validity bits corresponding to the cache line are all set to the predefined value, the eviction component to send the evicted data to the main memory.

11. (Original) The apparatus of claim 10 in which cache lines are disposed within a write cache memory of a computer chipset.

12. (Currently amended) The apparatus of ~~claim 11~~ claim 30 in which the cache coherent protocol comprises at least one of a modified-exclusive-invalid (MEI) protocol and modified-exclusive-shared-invalid (MESI) protocol.

13. (Currently amended) A method comprising:

receiving write transactions associated with write data to be written to a main memory;

storing the write data into portions of a single cache line of a cache memory ~~that complies with a cache coherent protocol~~; and

evicting the write data from the cache line when the cache line is full of write data according to stored validity information.

14. (Currently amended) The method of claim 13, further comprising writing the evicted bytes of data to ~~a main~~ the main memory.

15. (Previously Presented) The method of claim 13, further comprising setting validity bits to a predefined value when respective portions of the cache line is written in full with write data.

16. (Original) The method of claim 13 in which the write transactions are sent from an input/output device.

17. (Original) The method of claim 16 in which each of the write transactions sent from the input/output device writes a first number of data bytes to one of the cache lines, and the eviction component evicts a second number of data bytes in one eviction operation, the first number being less than the second number.

18. (Currently amended) Apparatus comprising:

a computer chipset comprising a cache memory to store write data sent from an input/output device, ~~the cache memory complying with a cache coherent protocol,~~ and a mechanism to evict the write data from the cache memory when a set of predefined conditions are met.

19. (Previously Presented) The apparatus of claim 18 in which the cache memory also stores additional write data sent from an additional input/output device, and the mechanism also to evict the additional write data from the cache memory when the set of predefined conditions are met.

20. (Currently amended) The apparatus of ~~claim 18~~ claim 33 in which the cache coherent protocol comprises at least one of a modified-exclusive-invalid (MEI) protocol and modified-exclusive-shared-invalid (MESI) protocol.

21. (Previously Presented) The apparatus of claim 18 in which the input/output device initiates write transactions to send the write data, and the mechanism is to combine the write data so that the number of eviction operations performed to evict the write data from the cache memory is less than the number of write transactions initiated by the input/output device.

22. (Original) A method comprising:
initiating write transactions by an input/output device to write data;
writing the data into a cache memory;
evicting the data from the cache memory; and
writing the data into a main memory.

23. (Currently amended) The method of claim 22 in which the cache memory contains cache lines to store data, each cache line corresponding to consecutive addresses in the main memory.

24. (Original) The method of claim 23 in which each cache line has multiple portions, each portion corresponding to a validity bit that tracks the status of the corresponding portion.

25. (Original) The method of claim 24 in which the validity bit is set to a predetermined value responsive of the number of bytes of data written into the corresponding portion.

26. (Original) The method of claim 25 in which the evicting the data from the cache memory comprises evicting the data when the validity bits corresponding to a cache line are all set to a predefined value.

27. (Currently amended) The apparatus of ~~claim 1~~ claim 29 in which the cache coherent protocol comprises at least one of a modified-exclusive-invalid (MEI) protocol and modified-exclusive-shared-invalid (MESI) protocol.

28. (Previously Presented) The method of claim 22 in which writing the data into the cache memory comprises writing the data into the cache memory complying with a cache coherent protocol.

29. (New) The apparatus of claim 1 in which the cache memory complies with a cache coherent protocol.

30. (New) The apparatus of claim 10 in which the cache memory complies with a cache coherent protocol.

31. (New) The method of claim 13 in which the cache memory complies with a cache coherent protocol.

32. (New) The method of claim 13, further comprising reading a segment of data from the main memory if the write data to be written to the main memory do not correspond to a cache line address of the cache line, a portion of the segment of data having the same addresses as the data to be written to the main memory.

33. (New) The apparatus of claim 18 in which the cache memory complies with a cache coherent protocol.